Q.P. Code: 16EC408 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations March 2021

COMPUTER ORGANIZATION AND ARCHITECTURE

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Demonstrate how the Compatibility between CPU & Bidirectional IO components are devised using its interfacing modules?	6M
	b	Construct and explain the 2-dimensional organization of 8x2 ROM Chip.	6M

OR

2	a	Identify the crucial features to design the instruction set architecture for a specific purpose processor.	6M
	b	List out the features of different levels in computer programming languages.	6M

UNIT-II

3	a	With a neat schematic, explain the steps involved in fetch and decode phases using register transfer instructions.	6M
	b	Illustrate the phases of Interrupt Cycle with a neat flowchart.	6M

OR

4	a	Write the basic instruction formats for IO, Register & Memory Reference instructions.	6M
	b	Implement hardware for multiplying Two fixed- point binary numbers in signed-magnitude representation along with its flowchart.	6M

UNIT-III

5	a	Design and implement 4-bit Arithmetic unit which performs ADD, ADD with carry, SUB, Sub with borrow, Increment and decrement operations.	8M
	b	Demonstrate the general configuration of Micro programmed Control unit with a neat block diagram.	4M

OR

6	a	Tabulate the logical and shift micro operations with its RTL notations.	6M
	b	Explain about address sequencing in control memory with neat diagrams.	6M

UNIT-IV

7	a	Explain the mechanism involved in Magnetic Disks and Magnetic Tapes.	6M
	b	With practical Examples, Explain the connection of I/O bus to input-output devices and it Specifications.	6M

OR

8	a	Illustrate the mapping process involved in transformation of data from main to Cache memory.	6M
	b	Explain Daisy-Chaining priority & Parallel priority Interrupt with its hardware diagram.	6M

UNIT-V

9	a	Demonstrate the pipeline organization for following example $A_i*B_i+C_i$ for i =1,2,3,…	8M
	b	Differentiate tightly coupled and loosely coupled multiprocessors.	4M

OR

10	a	With examples, Explain four segment CPU pipeline and Timing of instruction pipeline.	6M
	b	Illustrate serial & parallel arbitration produces in a shared multiprocessor environment.	6M

***** END *****